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Docket No.: 49657-274 PATENT

GP2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Eiji HASUNUMA, et al.

Serial No.: 09/227,935

Filed: January 11, 1999

Group Art Unit: 2811

Examiner: S. Loke

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEROF

TRANSMITTAL OF APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed June 6, 2000. Please charge the Appeal Brief fee of $300.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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TABLE OF CONTENTS

Page

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#15
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In re Application of :

Eiji HASUNUMA, et al. :

Serial No.: 09/227,935 : Group Art Unit: 2811

Filed: January 11, 1999 : Examiner: S. Loke

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEROF

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

This Brief is submitted pursuant to the appeal of the non-final rejection of claims 1, 2 and 4, filed June 6, 2000. The claims on appeal have been twice rejected.

REAL PARTY IN INTEREST

The real party in interest in this application is Mitsubishi Denki Kabushiki Kaisha.

RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are believed to affect or be affected by a decision in this appeal.

STATUS OF CLAIMS

All pending claims 1, 2 and 4 stand under final rejection.

STATUS OF AMENDMENTS

A post-final Office Action Amendment was filed April 7, 2000. An Advisory Action, dated April 18, 2000, indicates that this Amendment will be entered upon filing an appeal. It is presumed, therefore, that the Amendment has been entered of record and is appropriate for consideration in this appeal.

SUMMARY OF INVENTION

The present invention is related to integrated semiconductor device structure. The inventive structure is an improvement upon the prior art device depicted in Fig. 15. Depicted therein is a memory cell, one of a plurality of adjacent cells integrated into the device. A transistor, having source/drain regions 6 and gate 5, is formed at the surface of substrate 1. Capacitor 200 comprises elements 13-15 that are formed on and above the substrate surface, with storage node 13 extending beneath the substrate surface. P type isolation region 3 isolates the cell elements within the substrate. Oxide film 2 isolates pairs of adjacent cell elements. Storage node 13 extends through the oxide film 2 into the substrate. An adjacent cell on each side of the illustrated cell comprises the same element structure, although in mirror image so that a pair of adjacent cells can share source/drain regions and the same bit line connection 9, thereby obtaining economy of chip integration. With this arrangement, the storage node of the cell to left of the illustrated cell extends through the same illustrated oxide film 2. N type impurity region 12 is diffused in the substrate in the vicinity of the lower end of contact hole 10a in order to lower the impurity concentration of the p type isolation region 3 therebeneath and to attain electrical contact between the storage node 13 in contact hole 10a and the source/drain region 6.

The improvement of the present invention overcomes problems that applicants have recognized can occur from the fabrication of the prior art device described above. The isolation region 3 is provided at a position relatively deep from the surface of the silicon substrate 1. When the n type

impurity is introduced to silicon substrate 1 at relatively high energy to form the impurity region 12 to the depth of isolation region 3, the impurity is likely to spread to an undesirable extent in the lateral direction, especially at the vicinity of the substrate surface. As seen in Fig. A in the attached appendix, the width of the impurity in the lateral direction can attain an extent such as to cause adjacent impurity regions 12 to come in contact with each other, thereby short-circuiting storage nodes of adjacent transistors. One way of avoiding this result is to increase the distance between adjacent cells at the cost of integration efficiency. Another alternative is to reduce the diameter of the opening of the contact hole 10a used for introducing the n type impurity into the silicon substrate 1, thereby narrowing the lateral extent of the impurity region. Provision of framing film 11 in the hole, and removal thereof in a cleaning step, limits the amount by which the diameter of the opening of contact hole 10a can be reduced.

In the present invention (illustrated in Fig. 1) a framing film 51 is provided, which is not removed in a cleaning step, in order to reduce the diameter of the opening of contact hole 10a. To attain electrical connection between the storage node 13 in contact hole 10a with the source/drain region 6, impurity is first introduced using contact hole 10a before provision of framing film 51, so that impurity region 50 (the claimed second impurity region portion) is formed. Introduction of the impurity here need not be so extensive as to reach isolation region 3, and therefore, impurity introduction is possible with low energy. This suppresses unnecessary lateral extension of the impurity.

Thereafter, to reduce the impurity concentration in the p type isolation region 3, impurity is introduced using the contact hole 10a after framing film 51 has been provided, to form impurity region 52 (the claimed first impurity region portion). As the isolation region 3 is provided at a position relatively deep from the surface of silicon substrate 1, introduction of the impurity here requires high

energy. The area of opening to introduce the impurity, however, is small here, and therefore, undesirable lateral extension of the impurity is suppressed. As a result, adjacent first impurity regions 52 are not brought into contact with each other as shown in appended Fig. B.

Reference is made to the specification for a more detailed description of the present invention. Claim 1, the sole independent claims, is presented below with elements read on drawing figures, as urged in MPEP 1206.

1. A semiconductor device, comprising:

a semiconductor substrate (1, Fig. 1) having a main surface;

an element isolating region (2) for defining an element forming region on the main surface of said semiconductor substrate;

an isolation region (3) provided in a strip-shape and having a peak impurity concentration at a prescribed depth position from the main surface of said semiconductor substrate;

a connection hole (10a) provided piercing through said element isolating region;

an anti-HF (hydrofluoric acid) side wall film (51) not etched by hydrofluoric acid, provided to cover a side wall of said connection hole at least near a lower end of said connection hole;

an interconnection layer (13) provided to fill an inner portion of said connection hole; and

an impurity region provided in said semiconductor substrate extending from the lower end of said connection hole to said isolation region, wherein said impurity region comprises a first impurity region portion (52) provided to connect said interconnection layer to said isolation region, and a second impurity region portion (50) provided near the lower end of said connection hole and connected to said interconnection layer.

As stated in the section of the Manual noted above, the claims are not to be limited to this embodiment by such reading.

ISSUE

Whether claims 1, 2 and 4 are unpatentable over the prior art embodiment of Fig. 15

(hereinafter "prior art Fig. 15") in view of Kuroda U.S. patent 5,825,059 (hereinafter "Kuroda") under 35 USC § 103(a).

GROUPING OF CLAIMS

The claims each contain specific individual recitations which, in context, are believed to warrant separate consideration for patentability.

ARGUMENT

Claims 1, 2 and 4 stand rejected as being unpatentable over the prior art embodiment of Fig. 15 in view of Kuroda under 35 USC § 103(a). The position of the Examiner is stated to be that the prior art Fig. 15 embodiment shows everything claimed except for an anti-HF side wall film. Kuroda's disclosure of a silicon nitride film 20 (Fig. 5) formed on a side wall of a contact hole has been relied upon to conclude that it would have been obvious to provide such film on the side wall of the contact hole of the structure of Fig. 15, purportedly to protect the interconnection layer. The first and second impurity region portions recited in claim 1 was held in the Advisory Action to be equivalent to the impurity region 12 of Fig. 15. The Office Action thus has recognized two differences between the prior art embodiment and the claimed structure: the lack of the anti-HF side wall film, and first and second impurity region portions.

In the application of a rejection under 35 U.S.C. §103, it is incumbent upon the Examiner to provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. ***Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.***, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***Stratoflex, Inc. v. Aeroquip Corp.***, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); ***In re Warner***, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). The Examiner should recognize that the fact that the prior art *could* be modified so as to result in the combination defined by

the claims would not have made the modification obvious unless the prior art suggests the desirability of the modification. ***In re Deminski***, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). In the absence of such a prior art suggestion for modification of the references, the basis of the rejection is no more than inappropriate hindsight reconstruction using appellant's claims as a guide. ***In re Warner***, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

Thus, the PTO is charged with the initial burden of identifying a source in the applied prior art for: (1) claim features; and (2) the realistic requisite motivation for combining applied references to arrive at the claimed invention with a reasonable expectation of successfully achieving a specific benefit. ***Smith Industries Medical Systems v. Vital Signs, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999).*** . Rejections under 35 U.S.C. §103 must be predicated upon facts, not assumptions. ***In re Freed, 425 F.2d 785, 165 USPQ 570 (CCPA 1970); In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967); In re Lunsford, 357 F.2d 385, 148 USPQ 721 (CCPA 1966).*** What may or may not be known in general does not establish the requisite realistic motivation. ***In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995).*** The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103 is not an abstract concept, but must stem from the applied prior art as a whole and have realistically impelled one having ordinary skill in the art to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. ***In re Newell, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989).***

It is submitted that the Examiner has not established that a person of ordinary skill in the art would have been led by a reading of Kuroda to consider this reference in the context of the structure of prior art Fig. 15 nor, even if so considered, would have been motivated to modify the prior art Fig. 15 embodiment to result in the specifically claimed invention. Prior art Fig. 15 employs an oxide framing film 11 on the side wall of the contact hole. Storage node 13 is in direct contact with the framing film.

Kuroda (Fig. 5) provides a hole for contact plug 22A to be connected with source/drain region 17. The hole, which does not pierce element isolation region 11, has a side wall lined with insulating film 20 and non-crystal silicon layer 21A to surround contact plug 22A. The Office Action does not specify the manner in which the side wall structure of prior art Fig. 15 is to be modified, nor identify what disclosure in Kuroda would have impelled modification. A general allegation in the Office Action that "it would have been obvious to have the silicon nitride film of Kuroda in Prior art because it protects the interconnection layer" does not explain why an artisan would have been led to believe that the prior art Fig. 15 contact hole would need, or derive benefit from, the vaguely described modification proposed in the Office Action.

Under long established precedent, all words in a claim must be considered in deciding the patentability of that claim against the prior art. ***In re Wilson***, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). Each word in a claim must be given its proper meaning, as construed by a person skilled in the art, and no word in a claim can be ignored. Where required to determine the scope of a recited term, the disclosure may be used. ***In re Barr***, 444 F.2d 588, 170 USPQ 330 (CCPA 1971).

It is submitted that the Office Action has not given appropriate consideration to subject matter required by the last paragraph of claim 1. This paragraph recites a first impurity region portion to connect the interconnection layer to the isolation region, and a second impurity region portion near the lower end of said connection hole and connected to the interconnection layer. While the Advisory Action appears to recognize that two impurity region portions have been recited, it is merely concluded, without further explanation, that these requirements are equivalent to the single impurity region 12 of prior art Fig. 15.

The recited two impurity region portions are supported in the disclosure by Fig. 1 and its description in the specification. The portions have configurations, identifiably distinct from each other,

and are formed by different steps in the manufacturing process. The recited first impurity region portion (52), which connects the interconnection layer to the deep isolation region, is formed by application of relatively high energy through a narrow opening in the contact hole. The recited second impurity region portion, which does not extend to the isolation region, is formed by application of relatively low energy through a wider opening in the contact hole. These steps are depicted in Figs. 9-12 and the accompanying description in the specification. The purpose for forming these two distinct impurity portions, described above, is to overcome a significant problem with the prior art Fig. 15 embodiment, *i.e.*, the likelihood that the single impurity region of Fig. 15 can extend to a width sufficient to short circuit adjacent capacitor storage nodes. It is the inventors of this application that have identified this problem.

It is submitted, therefore, that the single impurity region of prior art Fig. 15 is not equivalent to the two impurity region portions recited in claim 1. It is further submitted that the Office Action does not meet its burden to set forth why the Examiner believes the recited impurity region portions are equivalent to the single impurity region of prior art Fig. 15. Moreover, the Examiner's mere statement of his belief in equivalency is not sufficient to substitute for presentation of a rationale as to why a person of ordinary skill in the art would have been impelled to modify the prior art Fig. 15 device to form two distinct impurity region portions. That is, "equivalence" does not equate to obviousness if the artisan would not have found suggestion in the prior art to modify the prior art Fig. 15 embodiment to achieve the invention recited in the claim.

It is further submitted that one must not arbitrarily subdivide the single, unitary impurity region of the prior art Fig. 15 device into two region portions merely in order, thereby, to read on the claim language. The prior art Fig. 15 embodiment is not described as including two impurity region portions between the interconnect layer and the isolation region and the record has presented no reason why an

artisan considering that embodiment would have so interpreted the device. Motivation for such an interpretation would only be derived, improperly, from a hindsight study of the present application invention disclosure.

Claims 2 and 4 are dependent from claim 1 and further require that the side wall film is a nitride film (claim 2) or either a polysilicon film or amorphous silicon film (claim 4). None of the Office Actions has addressed these claim requirements. It is submitted that these claim requirements, prima facie, are additional bases for patentability. Claims 2 and 4, additionally, are urged to be patentable for their dependence from claim 1.

CONCLUSION

For the reasons advanced above, appellant respectfully urges that the rejection of claims 1, 2 and 4 as being unpatentable over prior art Fig. 15 in view of Kuroda under 35 USC § 103(a) is improper.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX

1. A semiconductor device, comprising:

a semiconductor substrate having a main surface;

an element isolating region for defining an element forming region on the main surface of said semiconductor substrate;

an isolation region provided in a strip-shape and having a peak impurity concentration at a prescribed depth position from the main surface of said semiconductor substrate;

a connection hole provided piercing through said element isolating region;

an anti-HF (hydrofluoric acid) side wall film not etched by hydrofluoric acid, provided to cover a side wall of said connection hole at least near a lower end of said connection hole;

an interconnection layer provided to fill an inner portion of said connection hole; and

an impurity region provided in said semiconductor substrate extending from the lower end of said connection hole to said isolation region, wherein said impurity region comprises a first impurity region portion provided to connect said interconnection layer to said isolation region, and a second impurity region portion provided near the lower end of said connection hole and connected to said interconnection layer.

2. The semiconductor device according to claim 1, wherein said anti-HF side wall film is a nitride film.

4. The semiconductor device according to claim 1, wherein said anti-HF side wall [firm] film is either a polysilicon film or an amorphous silicon film.

Explanatory Figures

Fig. A

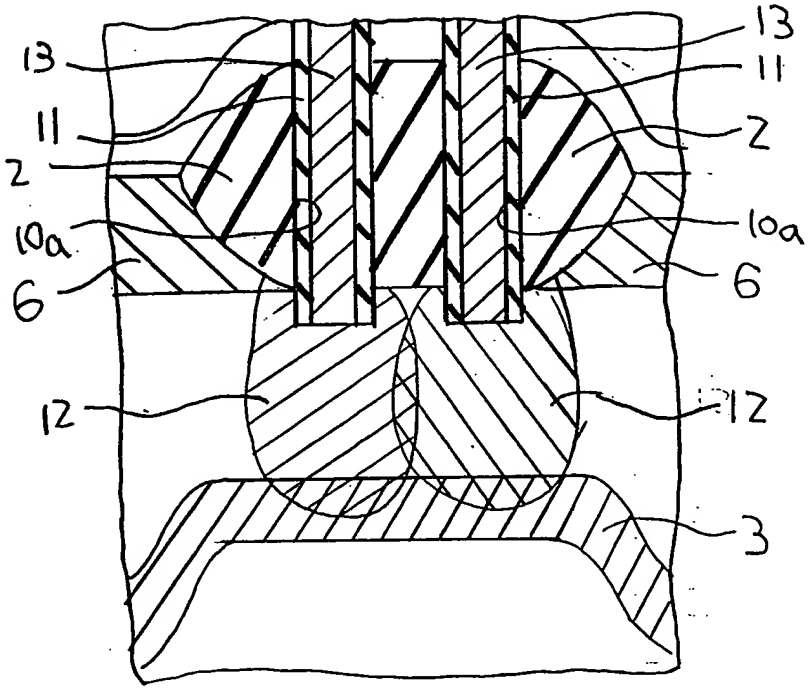

Fig. B